IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:	Confirmation No.: 8279
Arturo A. Rodriguez	Group Art Unit: 2483
Serial No.: 09/736,661	Examiner: An, Shawn S.
Filed: December 14, 2000	Docket No.: 60374.0052USU1/ CPOL 967732

For: System and Method for Adaptive Video Processing with Coordinated Resource Allocation

REPLY BRIEF UNDER 37 C.F.R. § 41.41

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is a Reply Brief in response to the Examiner's Answer dated January 13, 2011. The Examiner's Answer addresses Appellant's appeal brief filed on October 18, 2010.

I. STATUS OF THE CLAIMS

As set forth on page 2 of the Examiner's answer, claims 38, 53-55, 71-78, 80-82, and 85-89 remain pending and are the subject of this appeal. The Examiner's Answer maintains the rejections of the claims under 35 U.S.C. § 103(a) and generally repeats, on pages 3-10 of the Examiner's Answer, the arguments advanced in the final Office Action dated March 9 2010, in addition to the response to arguments presented in Section 10 ("Response to Arguments") on pages 10-11 of the Examiner's Answer. With regard to the substantive remarks of the Examiner's Answer, Appellant respectfully disagrees. Appellant addresses some issues raised in the Examiner's Answer, and continues to repeat, re-allege, and incorporate by reference the positions and arguments set forth in the Appeal Brief.

II. ARGUMENTS

Appellant addresses some of the rebuttal comments beginning on page 10 of the Examiner's Answer below. The omission of discussion pertaining to some issues raised in the Examiner's Answer should not be interpreted as an admission of the assertions made in the Examiner's Answer.

I. Rejection of claims 38, 53-55, and 89 under 35 U.S.C. § 103(a)

The Examiner's Answer provides the following rebuttal reproduced in part from pages 10-11 as follows (emphasis in original):

> The Appellant presents arguments that cited prior art references fail to disclose or describe:
>
> **i)** claims 38, 53-55, and 89, of which the recited **"*downscaling*"** occurs ***after*** the ***decompressed picture*** buffer (Appellants: pages 12, 21, 30, 38, and 48).
>
> However, after careful scrutiny of the cited prior art references, the Examiner must respectively[*sic*] disagree, and maintain the grounds of rejection for the reasons that follow.

> In response to argument **i)**, actually the only claimed limitation in claims 38, 53-55, and 89 that relates to the "downscaling" recites **"*transferring*** the set of retrieved reconstructed ***decoded/decompressed video frames*** to a display device while ***downscaling/scaling*** the video picture/frame(s) in transit to the display device.".[*sic*]
>
> In that aspect, Macinnins et al discloses a video decoder (Fig. 2, 50) to the video scaler (Fig. 2, 52), wherein the video scaler may perform both downscaling and upscaling of digital video and analog video as needed, and with analog and digital video input, either one may be scaled while other is displayed full size (col. 5, lines 65-66; col. 6, lines 1-9), wherein the analog video signal (as illustrated on Fig. 2) is used as an input signal to the video decoder (50) for an obvious decoding/decompression of the analog video signal, and subsequently transfer to the video scaler (52) for downscaling and/or upscaling of video frames, which is substantially the same/similar design as Applicant's decoder (Fig. 4, 81) to the video scaler (83).
>
> Therefore, Macinnins et al clearly discloses downscaling occurring after the decompressed video frames/pictures as discussed above.
> Furthermore, Boyce et al clearly teaches/illustrates ***downscaling (126)*** occurring ***after*** the ***decoded/decompressed picture*** buffer (202), wherein decoding is performed by IDCT (inverse discrete cosine transform) processing (124) and IQ (inverse quantization) processing (122).

Appellant respectfully disagrees with the above arguments. Initially, it is not clear from the Examiner's Answer why the transferring aspect is singled out when each of the claims and accompanying rationale supporting patentability in the Appeal Brief includes the memory aspect as well. Appellant believes that Federal case law mandates an "as a whole" requirement to the analysis, whereas the above picks and parts the claims to attempt to suit the rejection, without a clear understanding of the fundamental differences between the claims and the cited references as set forth in the Appeal Brief. For instance, the above-reproduced section of the Examiner's Answer appears to emphasize the video decoder 50 and the scaler 52, with the allegation "wherein the analog video signal (as illustrated on Fig. 2) is used as an input signal to the video decoder (50) for an obvious decoding/decompression of the analog video signal." (emphasis added) Appellant respectfully submits that *MacInnis* does not describe an analog signal that has been compressed as the input to the decoder. Indeed, how does one *decompress* an analog signal? Claim 38 requires a ***DHCT*** that operates in the resource-constrained mode by

"retrieving a set of ***reconstructed decompressed*** video frames from a memory component." Where is (or what is) the "***reconstructed decompressed*** video frames of the analog signal in *MacInnis*, and how is that seemingly paradoxical event actually achieved? Further, where is the ***memory component*** in *MacInnis*, which has been omitted from the explanation of the Examiner's Answer with regard to *MacInnis* and from which the claimed (e.g., claim 38) reconstructed decompressed video frames are retrieved? Appellant respectfully submits that these claimed elements do not exist in *MacInnis*.

In addition, there is reference in the above-reproduced section of the Examiner's Answer to a *digital signal*, but again, as thoroughly explained in the Appeal Brief, there is a retrieval from a memory component of reconstructed decompressed video frames, and then a downscaling in transit to a display device. As pointed out in the Appeal Brief (see, e.g., page 11), the citation to col. 6, lines 1-9 of *MacInnis* highlights the fundamental difference in structure between the claims and consequently Appellant's architecture (despite the claim to the contrary in the Examiner's Answer), and the function and architecture disclosed in *MacInnis*. It is also noted that the other independent claims of Appellant's claim sets refer to the decoded frames as corresponding to the compressed frames, in addition to memory aspects (e.g., for a DHCT), which simply raises the question how an analog signal reasonably applies, especially given at least one goal of *MacInnis* of downscaling prior to capture in memory.

In addition, the reference to *Boyce* is also unpersuasive. The reference to a buffer 202 in light of the fact that the buffer for decoded frames is explicitly disclosed as memory 118 is a misapplication of *Boyce* and a misunderstanding of the meaning of a memory component for storing reconstructed, decompressed frames. That is, col. 9, lines 61-65 of *Boyce* refers to the use of the "frame buffer 118" in post-sampling and decoding, whereas buffer 202 is described as follows (col. 10, , lines 10-18, Boyce, emphasis added):

> In the decoder 200, a small buffer 202, e.g., a buffer capable of storing the data corresponding to several lines of a video frame, in combination with a low pass filter 204, is used to couple the output of the IDCT circuit 124 to the input of the

> downsampler 126. The buffer 202 stores video data representing several scan lines of a picture which is then low pass filtered by the low pass filter 204 prior to downsampling to reduce the blockiness in the image that might otherwise result from the downsampling operation.

How is the storage of several lines representative of storage of "***a set of reconstructed decompressed video frames***?" Appellant respectfully believes it is not. Further evidence that the Examiner's Answer is misapplying the reference is found in col. 10, lines 44-45 of *Boyce*, which provides as follows:

> The received downsampled, decompressed video frames are stored in the frame memory 118.

Clearly, the decoding and sampling occur, and then the storage, and not in the manner as claimed.

For at least the reasons set forth above, and for the reasons incorporated herein by reference to the Appeal Brief, Appellant respectfully submits that the rejection be overturned and the claims allowed.

III. CONCLUSION

Based upon the foregoing discussion, the Appellants respectfully request that the Examiner's final rejection of claims 38, 53-55, 71-78, 80-82, and 85-89 be overruled and withdrawn by the Board, and that the application be allowed to issue as a patent with all pending claims.

No additional fee is believed to be due. However, any additional fee that may be due or required is authorized to be charged to deposit account no. 13-2725.

Respectfully submitted,

Date: March 11, 2011 By: /David Rodack/
David Rodack, Reg. No. 47,034

Merchant & Gould
P.O. Box 2903
Minneapolis, Minnesota 55402-9946
Telephone: 404.954.5049